ABSTRACT OF THE DISCLOSURE

A method of manufacturing a semiconductor wafer device, includes the steps of: (a) forming lower wiring patterns over a semiconductor wafer, the lower wiring patterns being connected to semiconductor elements in a circuit area; (b) forming an interlevel insulating film with a planarized surface over the semiconductor wafer, covering the lower wiring patterns and having a planarized surface; and (c) forming via conductors connected to the lower wiring patterns and wiring patterns disposed on the via conductors in the circuit area and conductor patterns corresponding to the wiring patterns in a peripheral area other than the circuit area, by embedding the via conductors, wiring patterns and conductor patterns in the interlevel insulating film, the conductive patterns being electrically isolated. The method can form a desired wiring structure and can prevent an increase of the percentage of defective devices in an effective wafer area.